conductive dummy interconnections provided in the plurality of layers so that every one of said conductive dummy interconnections is formed in a layer of said plurality of layers with at least one conductive interconnection; and

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 7-15 and 21-23 are pending in the present application. Claim 1 has been amended by the present amendment.

In the outstanding Office Action, Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. §103(a) as unpatentable over <u>JP 10-199882</u> (hereinafter <u>JP '882</u>) in view of <u>Lee</u>; Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. §103(a) as unpatentable over <u>JP '882</u> in view of <u>Ma</u>; and Claims 10-12 and 21-23 were allowed.

Applicant thanks the Examiner for the indication of allowable subject matter.

Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. §103(a) as unpatentable over <u>JP '882</u> in view of <u>Lee</u>. This rejection is respectfully traversed.

Amended Claim 1 is directed to a semiconductor device having interlayer insulating films, conductive interconnections provided in a plurality of layers, conductive dummy interconnections and a conductive dummy plug. The conductive dummy interconnections

are disposed such that every one of the conductive dummy interconnections is formed in a layer of the plurality of layers with at least one conductive interconnection.

Amended Claim 1 finds support in Figure 7 and recites more clearly an arrangement of the conductive dummy interconnections and the conductive interconnections.

In a non-limiting example, Figure 7 shows that every one of the conductive dummy interconnection 9a-9b is formed in the layer with at least one conductive interconnection 8a-8g.

The device in <u>JP '882</u> has a conductive dummy interconnection 12 (Figure 2), that is formed in a layer with no conductive interconnections 3, 5, 7 and 9. Therefore, the layer in which the conductive dummy interconnection 12 is formed, in <u>JP '822</u>, does not have at least one conductive interconnection. In other words, the conductive dummy interconnection 12 is alone in the layer.

Further, the outstanding Office Action states at page 2, item 2, that the device of <u>JP</u> <u>'882</u> includes conductive interconnections 3, 5, 7 and 9 and conductive dummy interconnections 3A, 5A, 7A, 9A and 12. Therefore, it is impossible that every one of the conductive dummy interconnections 3A, 5A, 7A, 9A and 12 (five dummy interconnections disposed in five different layers) have at least one conductive interconnection 3, 5, 7 and 9 (four interconnections) in a layer.

Furthermore, <u>Lee</u> does not teach or suggest every one of the conductive dummy interconnections being formed in a layer of a plurality of layers with at least one conductive interconnection.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. §103(a) as unpatentable over

<u>JP '882</u> in view of <u>Ma</u>. This rejection is respectfully traversed.

As discussed above, the device in <u>JP '882</u> does not teach or suggest every one of the

dummy interconnection being formed in a layer of a plurality of layers with at least one

conductive interconnection.

In addition, Ma does not teach or suggest this feature. Accordingly, it is respectfully

submitted independent Claim 1 and each of the claims depending therefrom are allowable.

Consequently, in light of the above discussion and in view of the present amendment,

the present application is believed to be in condition for allowance and an early and

favorable action to that effect is respectfully requested.

Finally, the attention of the Patent Office is directed to the change of address of

Applicant's representative, effective January 6, 2003:

Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

1940 Duke Street

Alexandria, VA 22314

Please direct all future communications to this address.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,

MAIER & NEUSTADT, P.C.

22850

Tel: (703) 413-3000

Attorney of Record

Registration No. 25,599

David A. Bilodeau

Registration No. 42,325

Fax: (703) 413-2220 GJM/DAB/RFF/smi

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Marked-Up Copy

Serial No: <u>09/612,298</u>

Amendment Filed on:

03/13/03

IN THE CLAIMS

Please amend Claim 1 as follows:

--1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films;

conductive dummy interconnections provided in the plurality of layers so that [each] every one of said conductive dummy [interconnection] interconnections is formed in a layer of said plurality of layers with at least one conductive interconnection; and

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.--